In the Claims

1. (currently amended) A phase/frequency comparator that generates a phase error responsive to a transition location signalapparatus ~~comprising:~~

~~a phase detecting stage that generates a result that represents an instantaneous phase difference; and~~

~~encoding circuitry coupled to the phase detecting stage;~~

~~wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value~~.

2. (currently amended) The apparatus of claim 7~~1~~, wherein the phase detecting stage further comprises:

a tapped delay line having a plurality of outputs and configured to receive a first signal; and

a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal,

wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and

wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value

3. (original) The apparatus of claim 2, further comprising:

an accumulator coupled to the encoding circuitry,

wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error.

4. (original) The apparatus of claim 3, wherein the encoding circuitry includes:

an edge detector coupled to the parallel latch; and

a weighted encoder,

wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch; and

wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal.

5. (original) The apparatus of claim 4, wherein the encoding circuitry includes:

a phase difference calculator configured to receive a lockpoint input,

wherein the phase difference calculator calculates a signed difference between the weighted numerical value and the lockpoint input; and

wherein the signed difference is presented to the accumulator as the numerical phase difference value.

6. (original) The apparatus of claim 4, wherein the weighted numerical value is presented to the accumulator as the numerical phase difference value.

7. (currently amended) The apparatus of claim 1~~, wherein the controlled oscillator is a numerically controlled oscillator.~~ further comprising:

a phase detecting stage that generates a result that represents an instantaneous phase difference; and

encoding circuitry coupled to the phase detecting stage;

wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value

8. (currently amended) The apparatus of claim 1, wherein the apparatus is ~~fabricated~~ implemented on a single monolithic integrated circuit.

9. (original) The apparatus of claim 8, wherein the apparatus is implemented in a field-programmable gate array on the single monolithic integrated circuit.

10. (currently amended) A phase locked loop comprising:

a ~~controlled~~ controllable oscillator; and

a phase/frequency comparator coupled to the ~~controlled~~ controllable oscillator such that an output of the ~~controlled~~ controllable oscillator is connected in a feedback loop to an input of the phase/frequency comparator and an output of the phase/frequency comparator is connected through a forward path to a control input of the controlled oscillator,

wherein the phase/frequency comparator includes:

a phase detecting stage ~~that generates a result that represents an instantaneous phase difference~~; ~~and~~

encoding circuitry coupled to the phase detecting stage; and

an accumulator coupled to the encoding circuitry.

~~wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value.~~

11. (original) The phase locked loop of claim 10, wherein the phase detecting stage further comprises:

a tapped delay line having a plurality of outputs and configured to receive a first signal; and

a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal,

wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and

wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value

12. (original) The phase locked loop of claim 11, further comprising:

an accumulator coupled to the encoding circuitry,

wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error.

13. (original) The phase locked loop of claim 12, wherein the encoding circuitry includes:

an edge detector coupled to the parallel latch; and

a weighted encoder,

wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch; and

wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal.

14. (original) The phase locked loop of claim 13, wherein the encoding circuitry includes:

a phase difference calculator configured to receive a lockpoint input,

wherein the phase difference calculator calculates a signed difference between the weighted numerical value and the lockpoint input; and

wherein the signed difference is presented to the accumulator as the numerical phase difference value.

15. (original) The phase locked loop of claim 13, wherein the weighted numerical value is presented to the accumulator as the numerical phase difference value.

16. (original) The phase locked loop of claim 10, wherein the forward path includes additional control circuitry.

17. (original) The phase locked loop of claim 10, wherein the controlled oscillator is a numerically controlled oscillator.

18. (currently amended) The phase locked loop of claim 10, wherein the phase locked loop is ~~fabricated~~ implemented on a single monolithic integrated circuit.

19. (original) The phase locked loop of claim 18, wherein the phase locked loop is implemented in a field-programmable gate array on the single monolithic integrated circuit.

20. (currently amended) A method comprising:

generating a snapshot of a first signal in response to receiving a second signal; and

mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal.

21. (original) The method of claim 20, further comprising:

combining the numerical phase difference value with a value in an accumulator to obtain a new accumulator value; and

presenting the new accumulator value as a result of a phase comparison.

22. (original) The method of claim 21, further comprising:

propagating the first signal through a tapped delay line;

latching outputs of the tapped delay line in a parallel latch in response to a transition in the second signal to obtain the snapshot of the first signal;

23. (original) The method of claim 20, further comprising:

detecting a location of an edge in the snapshot of the first signal; and

mapping the location into a weighted numerical value.

24. (original) The method of claim 23, further comprising:

comparing the weighted numerical value with a desired phase difference; and

presenting a difference between the weighted numerical value and the desired phase difference as the numerical phase difference value.

25. (original) The method of claim 20, further comprising:

controlling an output frequency of an oscillator using the result of the phase comparison.

26. (original) The method of claim 25, wherein one of the first signal and the second signal is an output of the oscillator.